METHOD FOR MITIGATING CHEMICAL VAPOR DEPOSITION PHOSPHORUS DOPING OXIDE SURFACE INDUCED DEFECTS

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to semiconductor fabrication. The present invention relates more particularly to a method for mitigating phosphorus doping oxide surface induced defects which occur following a chemical vapor deposition (CVD) semiconductor fabrication process.

2. Description of Related Art

[0002] Chemical vapor deposition (CVD) systems are well known. Chemical vapor deposition systems are commonly used to form thin films upon the surfaces of substrates during the fabrication of a wide variety of semiconductor devices. For example, chemical vapor deposition systems are used to form dopant, dielectric and passivation layers upon semiconductor wafers during the fabrication of light emitting diodes (LEDs) and integrated circuits (ICs).

[0003] During the chemical vapor deposition process, one or more reactant gases are introduced into a reactor chamber. The rate at which reactant gases are introduced into the reactor chamber can be carefully controlled. In this manner, the various layers needed to define the desired device are provided.

[0004] It is often desirable to form a phosphosilicate glass (PSG) passivation layer over a substrate, such as a silicon substrate, as well as any intermediate layers formed upon the substrate. The passivation layer protects the underlying layers from damage caused by environmental factors, such as ambient moisture and pollutants contained in the air. The passivation layer also provides some degree of mechanical protection.

[0005] However, although the use of such a phosphosilicate glass passivation layer has proven generally useful for its intended purposes, phosphosilicate glass passivation layers possess inherent deficiencies which detract from their overall effectiveness and desirability. For example, after annealing the phosphosilicate glass layer, phosphorus atoms tend to migrate toward the outer or upper surface of the phosphosilicate glass layer. These phosphorus atoms then react with ambient

moisture to undesirably affect the formation of defects in the phosphosilicate glass layer. These defects may facilitate the entry of harmful ambient substances into the layers below, thus mitigating the effectiveness of the phosphosilicate glass layer.

[0006] As such, although the prior art has recognized, to a limited extent, the problem of forming an adequate and reliable passivation layer upon semiconductor devices during the chemical vapor deposition process, the proposed solutions may not have, to date, been altogether effective in providing a satisfactory remedy. Therefore, it may be desirable to form a passivation layer which is resistant to defect formation due to the effects of ambient moisture upon phosphorus atoms therein, so as to provide a passivation layer having enhanced effectiveness.

BRIEF SUMMARY OF THE INVENTION

[0007] While the apparatus and method has or will be described for the sake of grammatical fluidity with functional explanations, it is to be expressly understood that the claims, unless expressly formulated under 35 USC 112, are not to be construed as necessarily limited in any way by the construction of "means" or "steps" limitations, but are to be accorded the full scope of the meaning and equivalents of the definition provided by the claims under the judicial doctrine of equivalents.

[0008] The present invention specifically addresses and tends to alleviate the above mentioned deficiencies associated with the prior art. More particularly, according to one aspect the present invention comprises a method for mitigating defect formation in a phosphosilicate glass layer, wherein the method comprises forming an oxide cap upon the phosphosilicate glass layer via a chemical vapor deposition process.

[0009] According to another aspect, the present invention comprises a method for mitigating defect formation in a passivation layer of a semiconductor device, wherein the method comprises forming a glass layer upon a substrate and forming a cap oxide layer upon the glass layer.

[0010] According to another aspect, the present invention comprises a wafer comprising a substrate, a glass passivation layer covering at least a portion of the substrate, and a cap oxide layer formed upon at least a portion of the glass passivation layer.

[0011] According to another aspect, the present invention comprises a die comprising a substrate, a glass passivation layer covering at least a portion of the substrate, and a cap oxide layer formed upon at least a portion of the glass passivation layer.

[0012] According to another aspect, the present invention comprises a semiconductor device comprising a substrate, a glass passivation layer covering at least a portion of the substrate, and a cap oxide layer formed upon at least a portion of the glass passivation layer.

[0013] These, as well as other aspects and advantages of the present invention, will be more apparent from the following description and drawings, wherein like elements are referenced by like numerals. It is understood that changes in the specific structure shown and described may be made within the scope of the claims, without departing from the spirit of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The invention and its various embodiments can now be better understood by turning to the following detailed description of the preferred embodiments which are presented as illustrated examples of the invention defined in the claims. It is expressly understood that the invention as defined by the claims may be broader than the illustrated embodiments described below.

[0015] Figure 1 is a fragmentary cross-sectional view of a silicon substrate having a phosphosilicate glass layer formed thereon according to contemporary methodology;

[0016] Figure 2 is a fragmentary cross-sectional view of the silicon substrate and phosphosilicate glass layer of Figure 1, showing the migration of phosphorus atoms toward the upper surface of the phosphosilicate glass layer;

[0017] Figure 3 is a fragmentary cross-sectional view of the silicon substrate and phosphosilicate glass layer of Figure 2, showing ambient moisture reacting with the migrated phosphorus atoms to cause defect formation in the phosphosilicate glass layer;

[0018] Figure 4 is a fragmentary cross-sectional view of a silicon substrate having a phosphosilicate glass layer formed thereon and also having a cap oxide layer formed upon the phosphosilicate glass layer according to the present invention;

[0019] Figure 5 is a fragmentary cross-sectional view of the silicon substrate, phosphosilicate glass layer, and cap oxide layer of Figure 4, showing the migration of phosphorus atoms toward the upper surface of the phosphosilicate glass layer; and

[0020] Figure 6 is a fragmentary cross-sectional view of the silicon substrate, phosphosilicate glass layer, and cap oxide layer of Figure 5, showing ambient moisture not reacting with the migrated

phosphorus atoms because the phosphosilicate glass layer is protected from the ambient moisture by the cap oxide layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] Reference will now be made in detail to the presently preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Illustrated embodiments described herein are presented by way of example and not by way of limitation, and the process steps and structures described herein do not cover a complete process flow. The present invention may be practiced in conjunction with various integrated circuit fabrication techniques that are conventionally used in the art, and only so much of the commonly practiced process steps are included herein as are necessary to provide an understanding of the present invention.

[0022] The present invention provides a method for mitigating defect formations in a phosphosilicate glass layer, wherein the method includes forming an oxide cap upon the phosphosilicate glass layer via a chemical vapor deposition process. In accordance with another aspect, a method for mitigating defect formation in a passivation layer of a semiconductor device comprises forming a glass layer on a substrate and forming a cap oxide layer on the glass layer.

[0023] The forming of a glass layer preferably comprises formation of a phosphosilicate glass layer. The substrate preferably comprises a silicon substrate. However, as those skilled in the art will appreciate, various other glass and substrate materials may likewise be suitable.

[0024] The substrate preferably has at least one semiconductor layer formed thereon. For example, the substrate may have a plurality of integrated circuits (IC's) or light emitting diodes (LED's) formed thereon. The substrate will typically comprises a wafer which is subsequently cut or diced into a plurality of individual die which are then used to fabricate semiconductor devices.

[0025] Forming the glass layer upon the substrate preferably comprises forming the glass layer via a chemical vapor deposition process. However, those skilled in the art will appreciate that various other processes may likewise be suitable.

[0026] Similarly, forming the cap oxide layer upon the glass layer preferably comprises forming the cap oxide layer via a chemical vapor deposition process. Again, those skilled in the art will appreciate that various other processes may likewise be suitable.

[0027] A chamber of the reactor within which the glass and cap oxide chemical vapor deposition processes are performed is preferably not opened or broken between the glass and cap oxide chemical vapor deposition processes. The ability to form the glass and cap oxide layers upon the substrate without having to break the chamber of the chemical vapor deposition reactor has several substantial advantages. For example, breaking the chamber between process can be an undesirably time consuming and costly process. Moreover, breaking the chamber can afford the potential for contaminating or otherwise damaging the semiconductors being processed therein.

[0028] Forming a cap oxide layer upon the glass layer preferably comprises forming an undoped oxide layer upon the glass layer. Forming a glass layer upon a substrate preferably comprises forming a phosphorus doped oxide film upon the substrate.

[0029] The glass layer and/or the cap oxide layer is preferably formed by a plasma enhanced chemical vapor deposition process, a sub-atmosphere chemical vapor deposition process, or an atmospheric ambient chemical vapor deposition process. Those skilled in the art will appreciate that various other processes may similarly be suitable for forming the glass layer and/or the cap oxide layer.

[0030] The cap oxide layer is preferably formed to have a thickness greater than 300 Angstroms. The phosphorus blocking capability of the cap oxide layer is preferably at least 11% by weight.

[0031] The cap oxide layer is preferably formed either via the use of SiH_4 and N_2O reacting gases or via the use of TEOS and O_2 reactant gases. Those skilled in the art will appreciate that various other gases may similarly be used to form the cap oxide layer.

[0032] The cap oxide layer process temperature is preferably between approximately 350°C and approximately 600°C. The glass layer process temperature is preferably between approximately 450°C and approximately 650°C.

[0033] Forming the cap oxide layer optionally comprises forming an inter-layer dielectric, an inter-poly dielectric and/or an inter-metal dielectric layer.

[0034] The present invention further provides various structures, such as a wafer including a substrate, a glass passivation layer covering at least a portion of the substrate, and a cap oxide layer formed on at least a portion of the glass passivation layer. In another aspect, a die is provided comprising a substrate, a glass passivation layer covering at least a portion of the substrate, and a cap oxide layer formed upon at least a portion of the glass passivation layer. In accordance with yet

another aspect, the present invention provides a semiconductor device having a substrate, a glass passivation layer covering at least a portion of the substrate, and a cap oxide layer formed upon at least a portion of the glass passivation layer.

[0035] Referring more particularly to the drawings, Figures 1-3 depict the process of undesirable defect formation in a phosphosilicate glass passivation layer formed upon a silicon substrate according to contemporary methodology.

[0036] With particular reference to Figure 1, a phosphosilicate glass layer 11 is formed upon a silicon substrate 12, such as via a chemical vapor deposition process. As discussed above, the phosphosilicate glass layer 11 defines a passivation layer which protects the underling semiconductor device(s) formed upon the substrate 12.

[0037] The substrate 12 as depicted in Figures 1-6 may depict the substrate defined by a wafer, the substrate of a die, or the substrate of a semiconductor device such as an integrated circuit or light emitting diode.

[0038] With particular reference to Figure 2, after the substrate 12 and the glass layer 11 are annealed, phosphorus atoms (designated by P) tend to migrate toward the upper surface of the glass layer 11 (as indicated by the upwardly pointing arrows).

[0039] With particular reference to Figure 3, typically after a period of days ambient moisture (designated by H_2O) reacts (as indicated by the diagonal arrows) with the phosphorus atoms that have migrated to the surface of the glass layer 11. This reaction tends to form undesirable defects in the glass layer 11 which can mitigate the glass layer's utility as a passivation layer and which may lead to failure of the semiconductor device.

[0040] Figures 4-6 depict a process of defect mitigation in a phosphosilicate glass passivation layer in accordance with an illustrated embodiment of the present invention, wherein a cap oxide layer is formed upon the phosphosilicate glass passivation layer.

[0041] Referring now to Figure 4, a cap oxide layer 14 is formed upon a phosphosilicate glass layer 11. As mentioned above, this cap oxide layer is preferably formed without opening or breaking the reactor chamber between the process of forming the phosphosilicate glass layer 11 and the process of forming the cap oxide layer 14.

[0042] Turning now to Figure 5, phosphorus atoms still tend to migrate toward the upper surface of the phosphosilicate glass layer 11 after the annealing process. However, such migration is

substantially mitigated from continuing into the cap oxide layer 14 as a result of the cap oxide layer 14.

[0043] Referring now to Figure 6, the cap oxide layer 14 substantially mitigates contact of ambient moisture with the migrated phosphorus atoms. Thus, reactions between such ambient moisture and the phosphorus atoms and the consequent formation of defects in the glass layer 11 are substantially mitigated.

[0044] The following table provides experimental data regarding testing of an embodiment of the present invention. Wafer number 1 was a control wafer which did not have a cap oxide layer and which had 15,924 defects one day after rapid thermal annealing. Wafer numbers 2-6 had a cap oxide layer and had between 19 and 62 defects one day after rapid thermal annealing.

Wafer	Purpose	P % Wt.	Cap Oxide Depth	Defects After Deposit	Defects After RTP	Defects After RTP + 1 Day
1	Control	8	W/0	18	22	15924
2	Cap oxide effect with P %	5	1KA	13	38	44
3		8	1KA	43	52	62
4		11	1KA	15	37	41
5	Cap oxide thickness effect	8	300 A	13	15	19
6		8	500 A	28	42	51

[0045] Wafers 2-4 were formed with different amounts of phosphorus doping (P% Wt.) while maintaining the cap oxide depth (Cap Oxide Depth) constant at 1 kAngstrom. Wafers 5 and 6 had different cap oxide depths while maintaining the amount of phosphorus doping constant at 8% by weight.

[0046] Defect scans were performed on the wafer immediately after the chemical vapor deposition process (Defects After Deposit), after rapid thermal annealing (Defects After RTP), and one day after rapid thermal annealing (Defects After RTP + 1 Day). The defect count is tabulated in each instance.

[0047] It is clear that all five of the cap oxide test wafers had far fewer defects than the control wafer one day after rapid thermal annealing.

[0048] The phosphosilicate glass layer, in combination with the cap oxide layer, may be used to achieve planarization of a substrate of an integrated circuit. That is, phosphosilicate glass and cap oxide may be selectively deposited upon the integrated circuit so as to tend to level or fill in low portions thereof. Thus, phosphosilicate glass and cap oxide may be used to form inter-layer dielectrics (ILDs) in accordance with the present invention.

[0049] A phosphosilicate glass layer, in combination with the cap oxide layer may find various other applications with respect to the formation of integrated circuits in accordance with the present invention. A phosphosilicate glass and cap oxide composite layer may, for example, be used as an inter-poly dielectric layer or inter-metal dielectric layer, as well as an inter-layer dielectric layer.

[0050] It is understood that the exemplary method described herein and shown in the drawings represents only presently preferred embodiments of the invention. Indeed, various modifications and additions may be made to such embodiments without departing from the spirit and scope of the invention. For example, the use of various processes other than chemical vapor deposition are contemplated. Thus, these and other modifications and additions may be obvious to those skilled in the art and may be implemented to adapt the present invention for use in a variety of different applications.